BEE 271 Digital circuits and systems

Spring 2017

Lab orientation

Nicole Hamilton

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Office hours by appointment
(I do not have an on-campus office.)

Education

- BS & MS EE, Stanford, 1973.
- MBA, Boston University, 1987.

Background

- Most of it as an entrepreneur selling a C shell I wrote for Windows.
- Also worked at IBM, Microsoft and RealNetworks.
- At Microsoft, I wrote the ranker and query language for the first release of what's now Bing.
- Here at UWB since 2013, initially as a Capstone advisor.

Download a free copy from my faculty page.

Lectures

Mondays and Wednesdays
5:45 pm to 7:45 pm
Beardslee 260

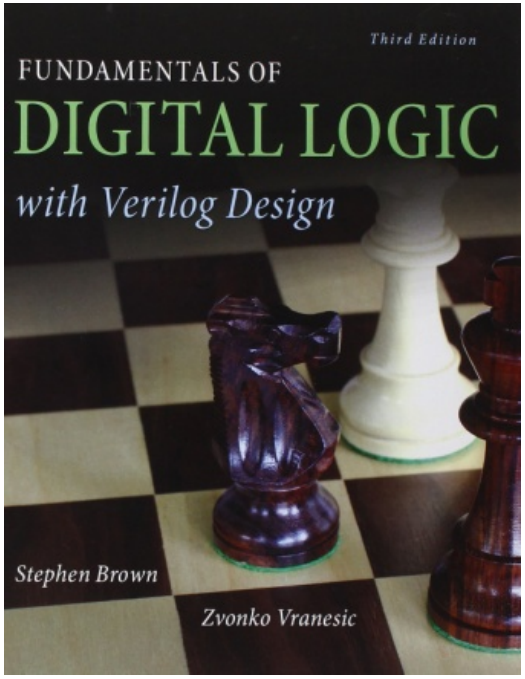
Labs

Mondays
3:30 pm to 5:30 pm
Beardslee 220

Topics

1. Combinatorial logic.
2. Synchronous sequential logic and finite state machines.
3. Verilog and FPGAs.

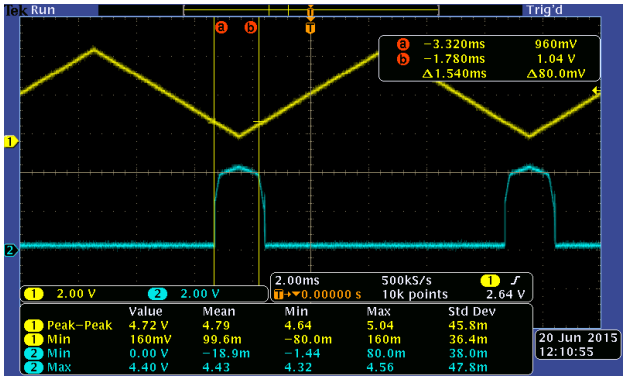
Required text



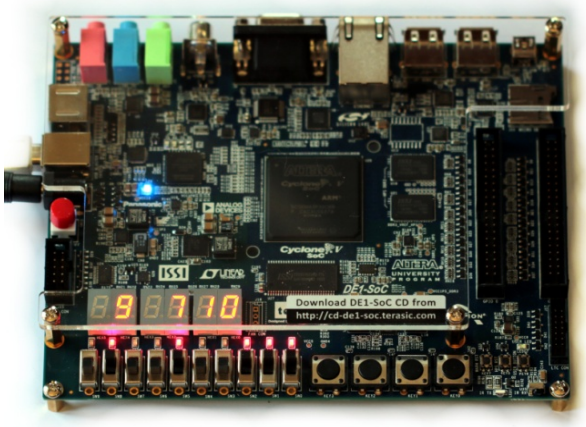
Fundamentals of Digital Logic with Verilog Design, Third Edition
Stephen Brown
Zvonko Vranesi
McGraw-Hill Education, 2013
ISBN 978-0073380544

You will need to read appendix A on the Verilog language.

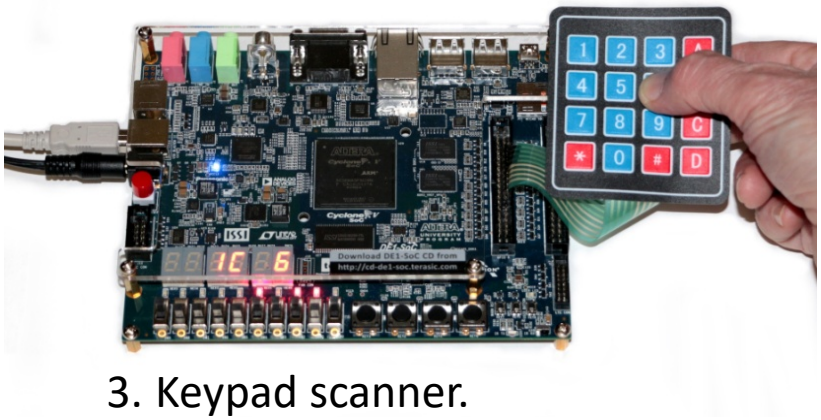
Four labs



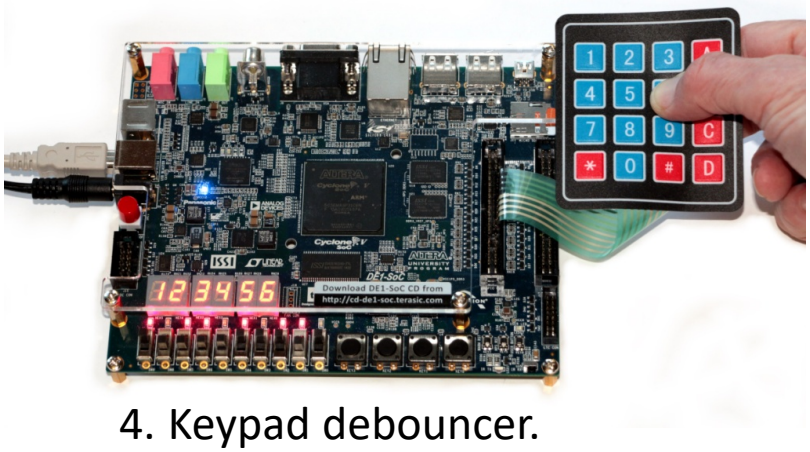
1. Digital logic devices.



2. Hex adding machine.

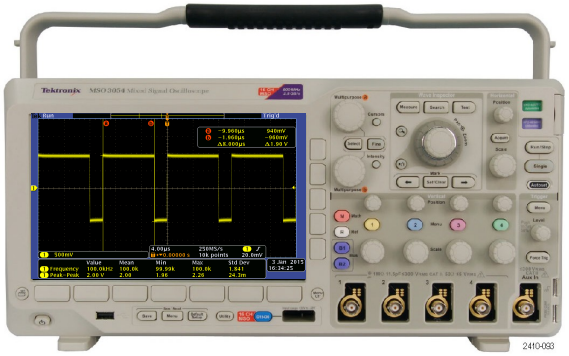


3. Keypad scanner.

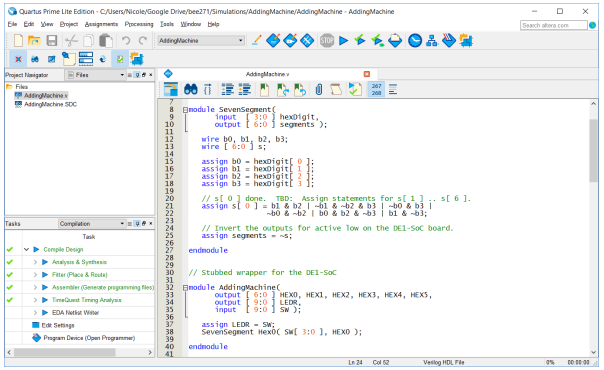


4. Keypad debouncer.

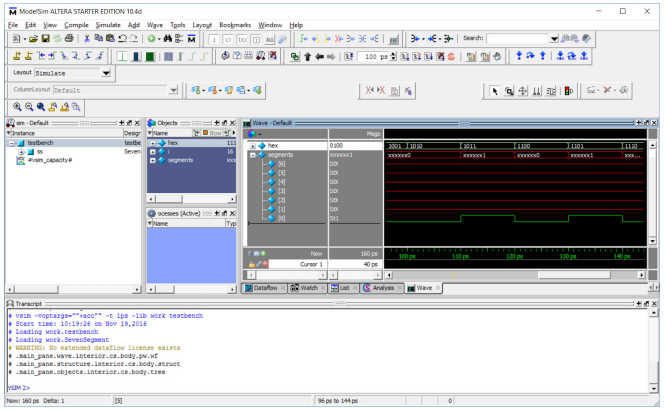
Four group exercises



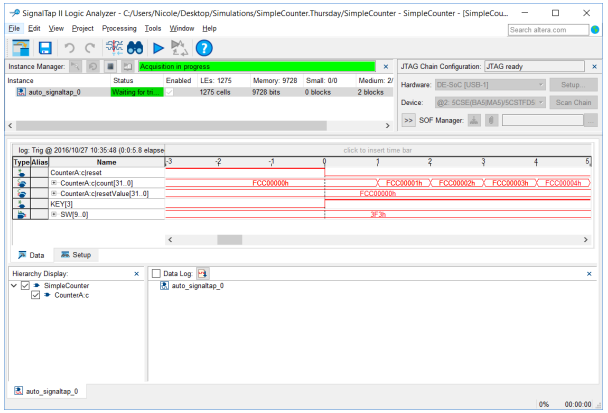
1. Use the lab instruments to measure switching thresholds.



2. Create and run a new Verilog project using Quartus.



3. Use the ModelSim simulator.



4. Use the SignalTap II logic analyzer.

Teams of 2 in the lab

1. No exceptions unless we have an odd number.
2. It is up to you to select your partner.
3. Both partners are expected to contribute equally to each lab.
4. My grading will assume you've done that, meaning you'll both get the same grade.
5. Each team should submit *only one* copy of each report but with both names on it.
6. To turn off the complaint from canvas, submit an otherwise blank sheet that gives your teammate's name.

Submissions

Only the first lab is a traditional EE lab assignment requires an actual report.

For the projects, you will be required to demo your design and submit your code as a .v (Verilog) or .sv (SystemVerilog) file plus any requested design notes as a PDF.

Lab reports

1. Reports may be typed or handwritten neatly *in ink* and submitted in PDF format or on paper.

2. I will not accept cellphone photographs of your work. If you submit a scan, it must have been made on an actual scanner.

3. I already have a copy of the assignment, so I do not need you to copy-and-paste it into your report.

4. I also do not need title pages with colorful backgrounds, boxes identifying who did what, a list of the standard lab instruments at each bench or anything else not called for in the assignment.

5. *I do need a **schematic** for each circuit you're discussing.*

Grading

1. I tend to count up the number of “things” a given lab is asking for and assign each a roughly equal value.

2. I never deduct points simply because your measured results didn’t perfectly match the expected.

3. I am *extremely* picky on reports, easy on projects. On labs, I give a lot of 40s and 50s to people who’ve never seen them before. On the projects, I’m more concerned that you make it work.

4. Each lab is only worth 5% of your grade, I do this to everyone and it all gets curved.

Come prepared

All but the first lab require a significant amount of prelab work.

But all you need to bring is a notebook, your laptop and a thumb drive.

Your lab kit contains everything else you need.

Lab kits

830-point (full-size) breadboard

Precut and preformed breadboard jumper wires

16-key numerical keypad

3-piece 20 cm multicolored 40-pin jumper wire “Dupont” ribbon cable set

Texas Instruments SN7400N Quad NAND or equivalent.

Texas Instruments SN7402N Quad NOR or equivalent.

Texas Instruments SN7404N Hex Inverter or equivalent.

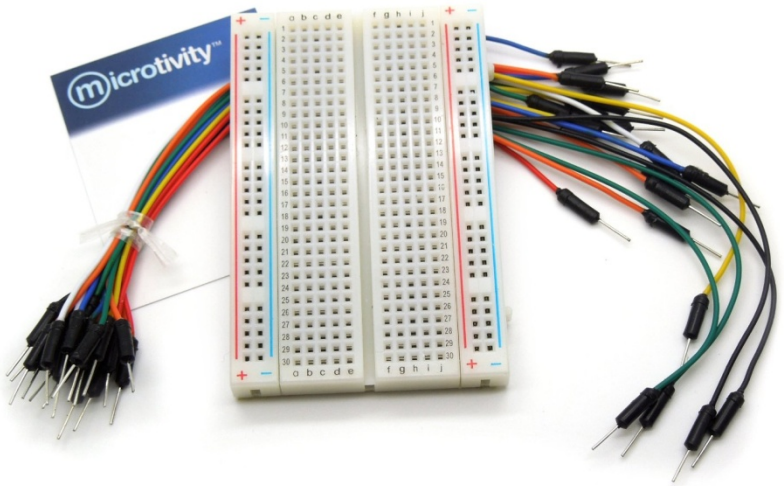
Texas Instruments SN74LS86AN Quad XOR or equivalent.

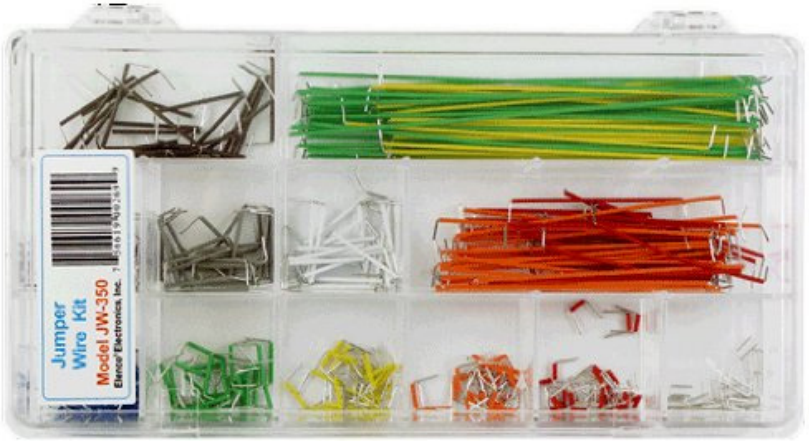
3 Generic 470 ohm, 1/4 watt, 5% resistors

4 Generic 10K ohm, 1/4 watt, 5% resistors

3 Generic red LEDs

Breadboards and wires





1. All the holes in a row are connected together.
2. Red is VCC (5 V), blue is ground. If a red or blue line is broken, it's disconnected at that point.
3. TTL chips are inserted straddling the trough in the middle and must have power.
4. Flexible wires are for going off the board.
5. Pre-formed wires are for making connections between places separated by specific numbers of holes on the board.
6. Don't rebend the pre-formed wires or use them to go off-board unless you want everyone to know you're a newbie.

Lab 1 Digital logic devices

BEE 271 Digital circuits and systems
Spring 2017
Lab 1: Digital logic devices[1]

1 Objectives

The purpose of this lab is to familiarize you with the characteristics of some simple TTL parts that implement basic digital logic functions and with the use of our lab instruments.

There are no previous core EE course requirements for this class, so it's perfectly okay if you've never used the lab instruments before and need help.

2 Transistor-transistor logic

Transistor-transistor logic (TTL) is a type of digital circuitry built using bipolar junction transistors (BJTs) and resistors. It's called transistor-transistor logic because both the logic function applied against the input and the amplification needed to drive the output are done with transistors, in contrast to earlier RTL and DTL technologies that used resistors or diodes to perform the logic function.

Figure 1 shows the TTL voltage levels for high and low states. Notice the standard provides a 0.4 V noise margin between the allowable input and output values.

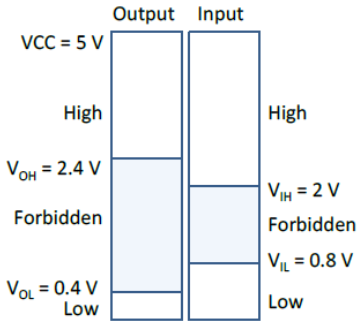


Figure 1. TTL voltage levels.

The most popular family of TTL components is the SN7400 series of small-scale integration (SSI) parts introduced by Texas Instruments in 1964, starting with the SN7400 quad 2-input NAND, originally in a metal package for the military, and in 1966, in a plastic DIP for commercial customers. There are now over 600 different parts in the SN7400 series and several variations on the internal circuitry offering a choice of speed and power trade-offs.

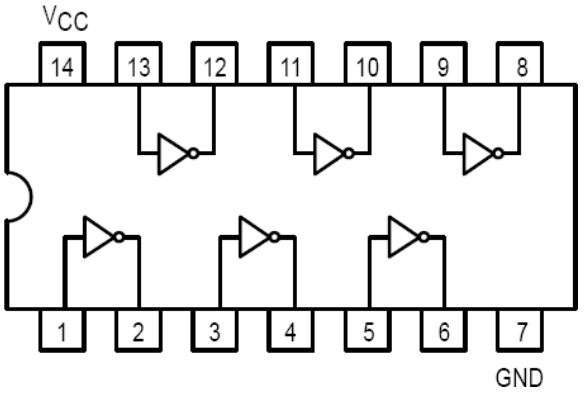
[1] This lab was written by Nicole Hamilton.

1

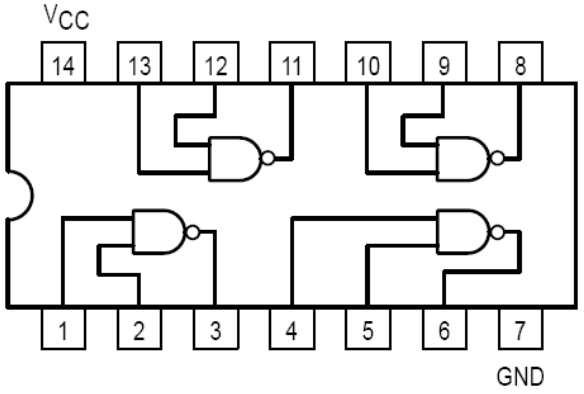
Learning objectives

1. Learn how to use our lab instruments.
2. Make a connection between Boolean algebra and the circuits we use to build things.
3. Learn how ones and zeros are represented as voltages and that circuits have propagation delays.
4. Create truth tables for inverter, NAND, NOR and XOR gates.
5. Observe what happens with feedback.
6. Explain some puzzling behavior.

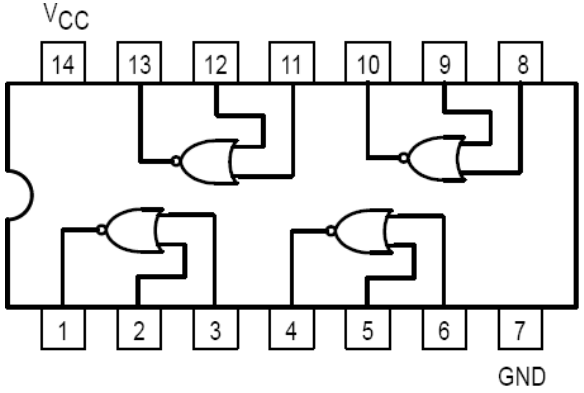
The TTL chips you'll characterize



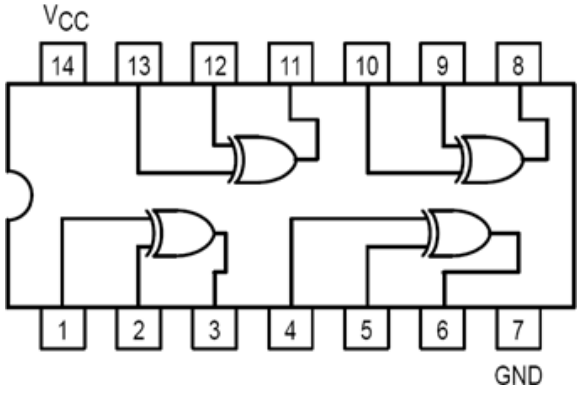
7404 Hex inverter



7400 Quad 2-input NAND

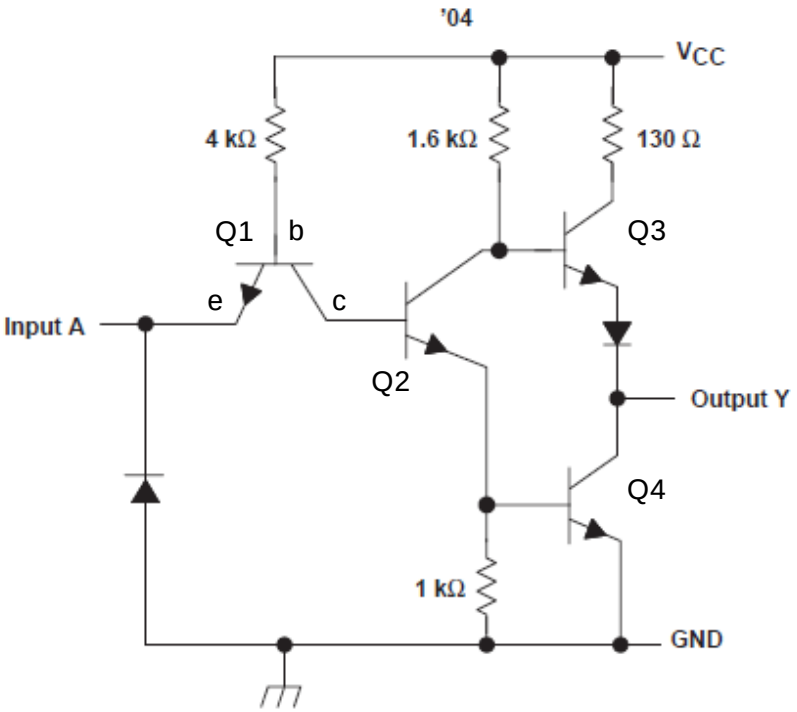


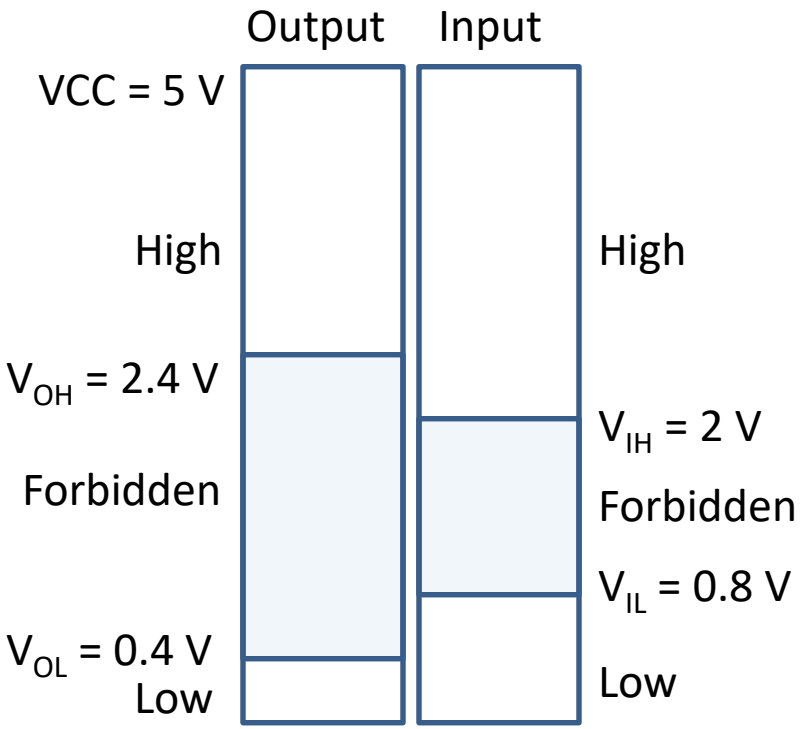
7402 Quad 2-input NOR



7486 Quad 2-input XOR

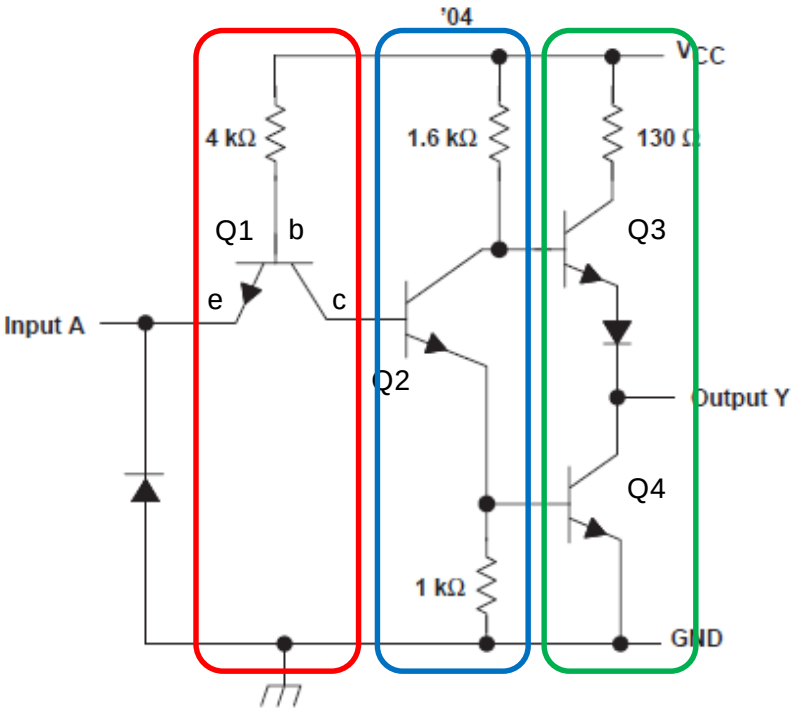
SN7400 Inverter





Circuit image source: Texas Instruments SN7400 datasheet

SN7400 Inverter

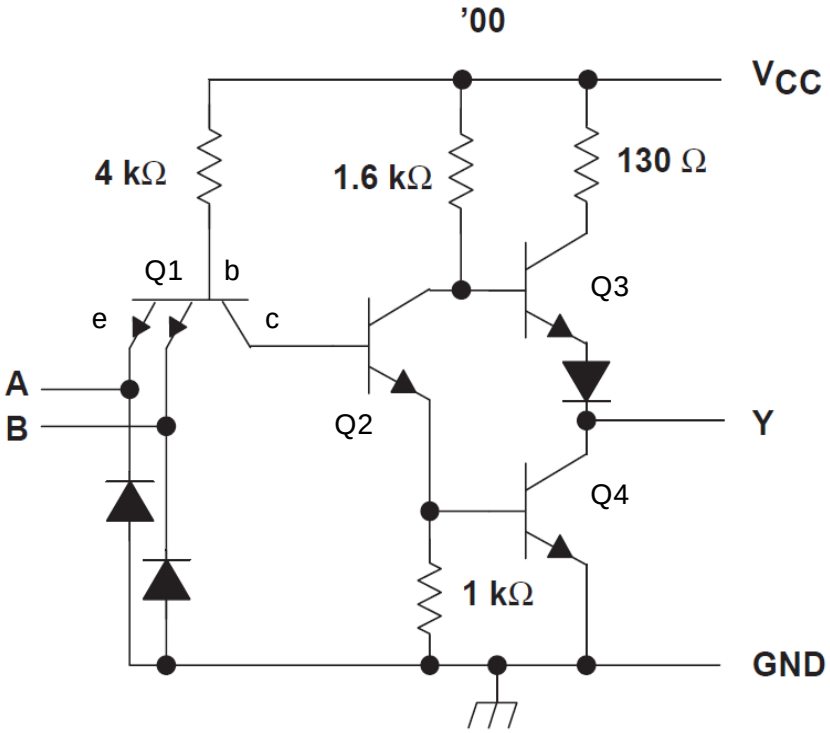


Three stages:

1. Non-inverting common base amplifier.
2. Inverting common emitter amplifier.
3. Non-inverting push-pull power amplifier.
4. If the input A is low, the output is high, otherwise low.

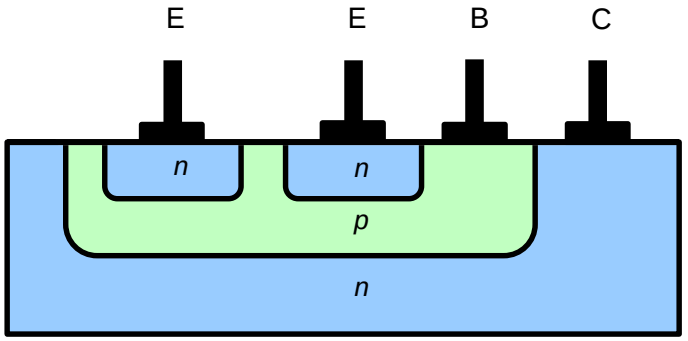
A transistor turns on when Vbe > 0.7 V, allowing current to flow from collector to emitter.

SN7404 NAND



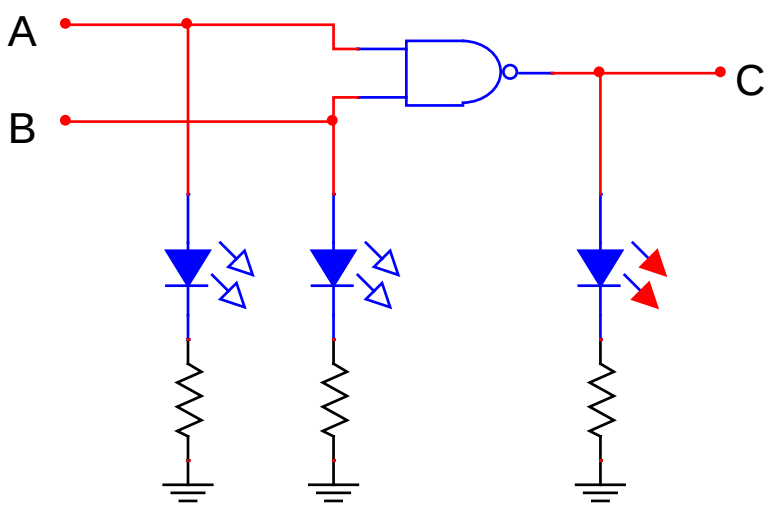
Input transistor Q1 fabricated with multiple emitters. If any Vbe > 0.7 V, the transistor turns on.

If either A or B is low, the output Y is high, otherwise low.



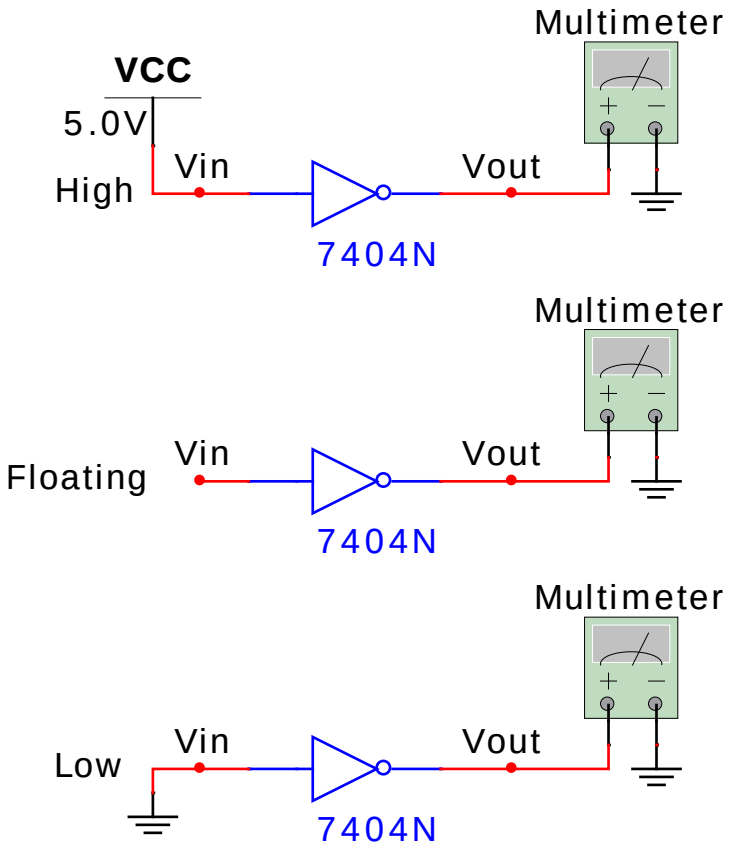
Circuit image source: Texas Instruments SN7404 datasheet

Truth tables

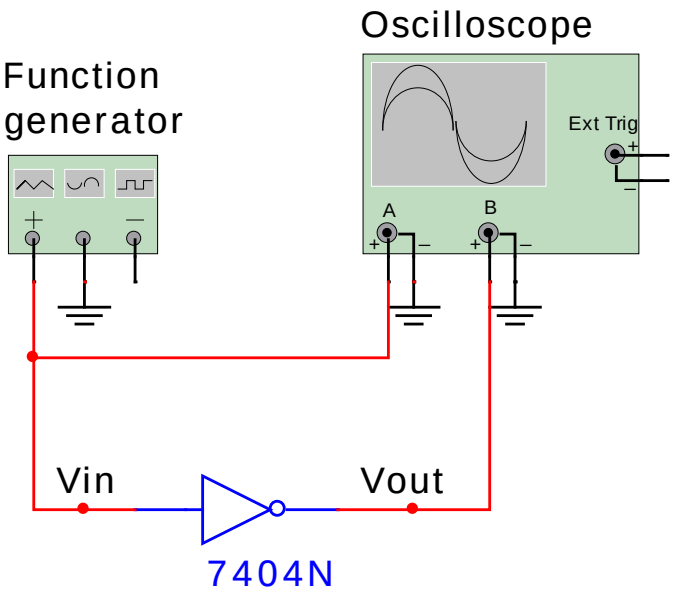


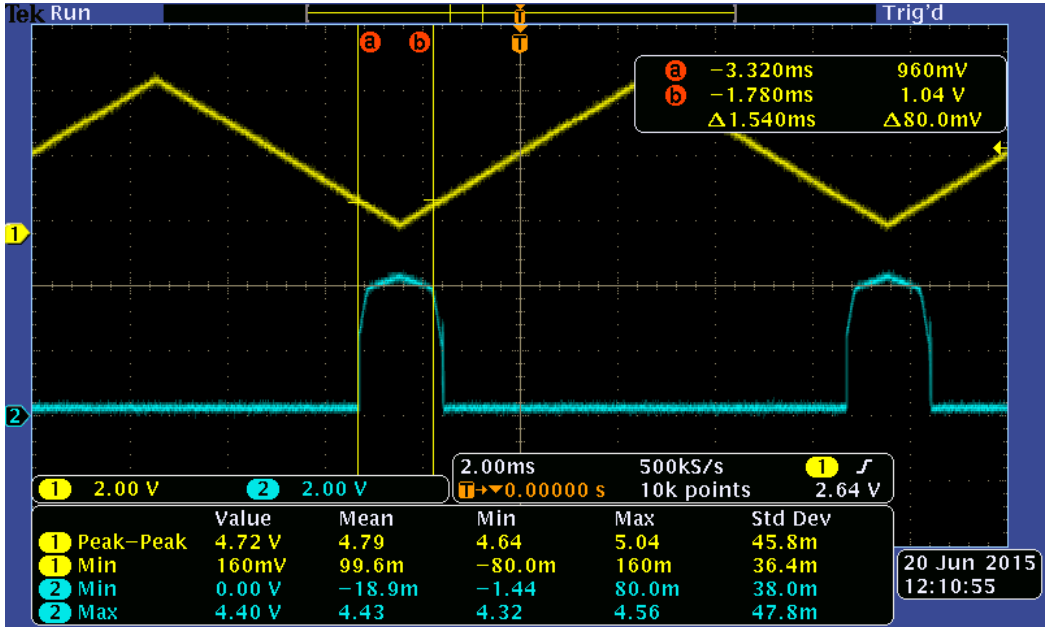
A	B	C
0	0	
0	1	?
1	0	
1	1	

Measuring output levels



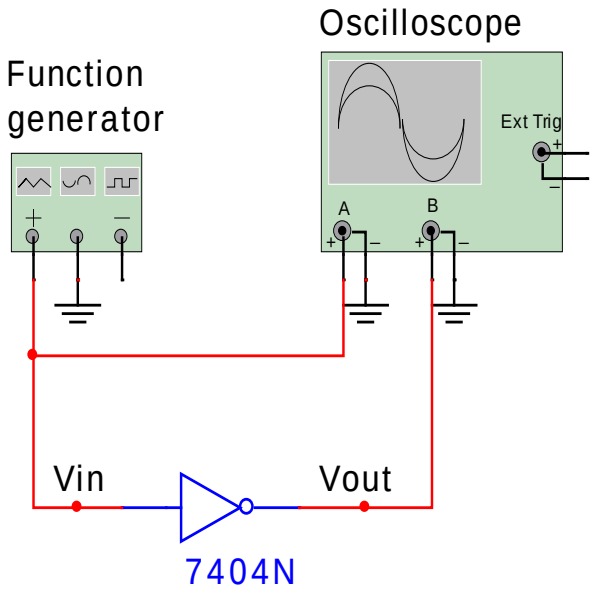
Switching thresholds

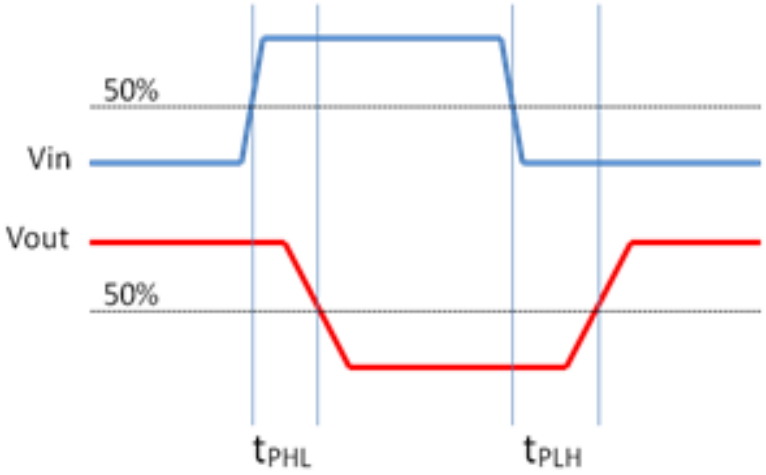


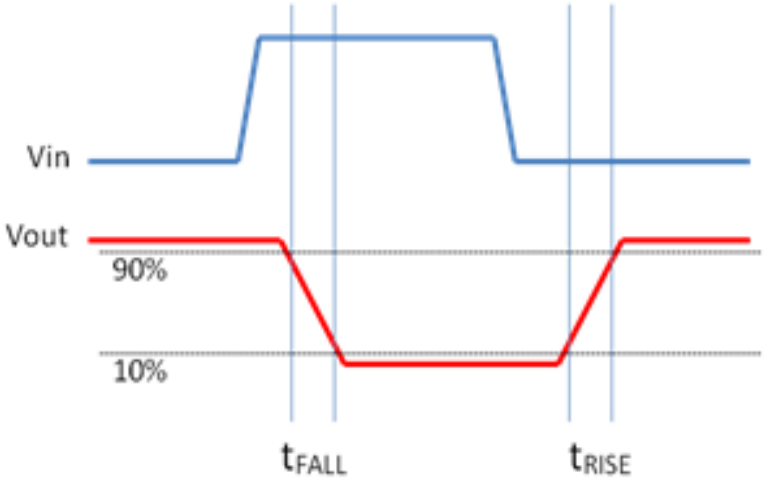


(We'll take this measurement today as a group.)

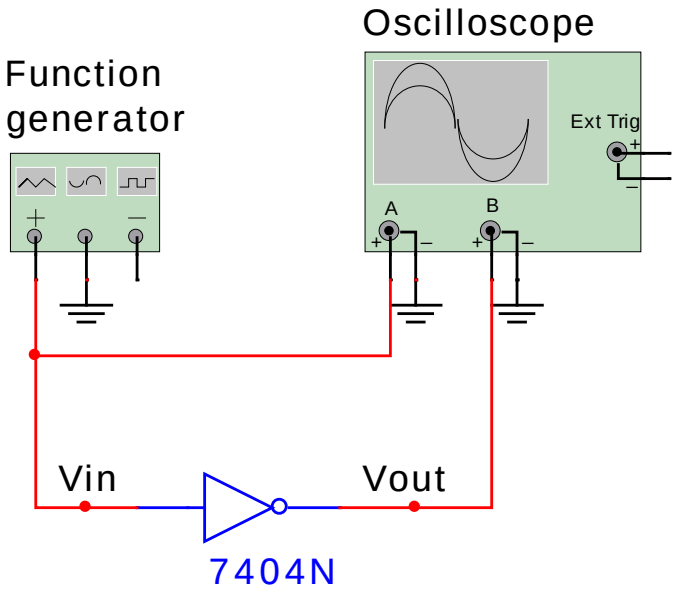
Measuring propagation and rise and fall times

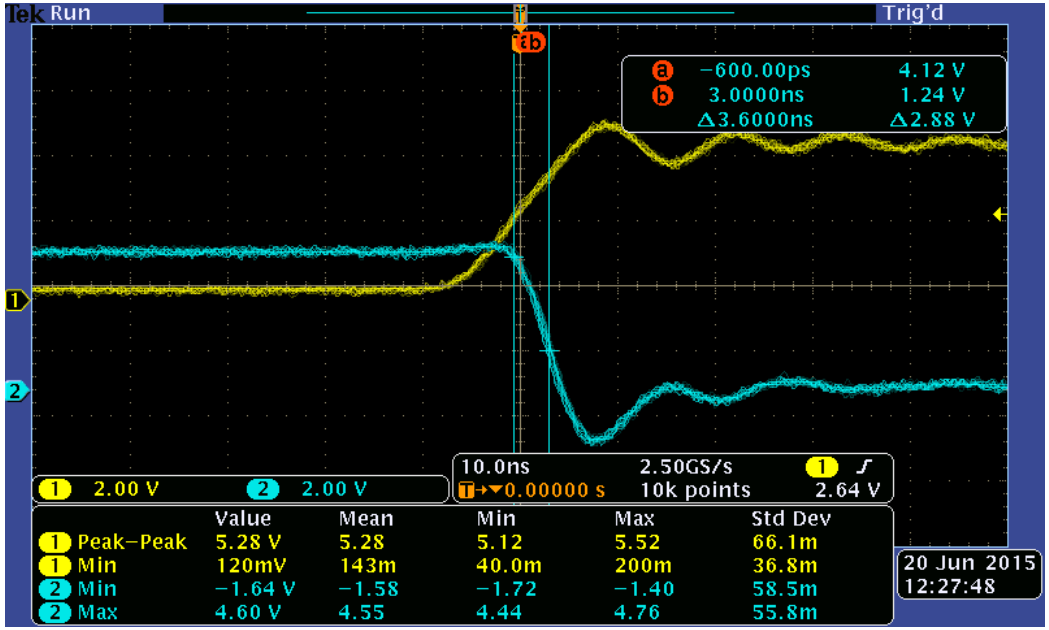






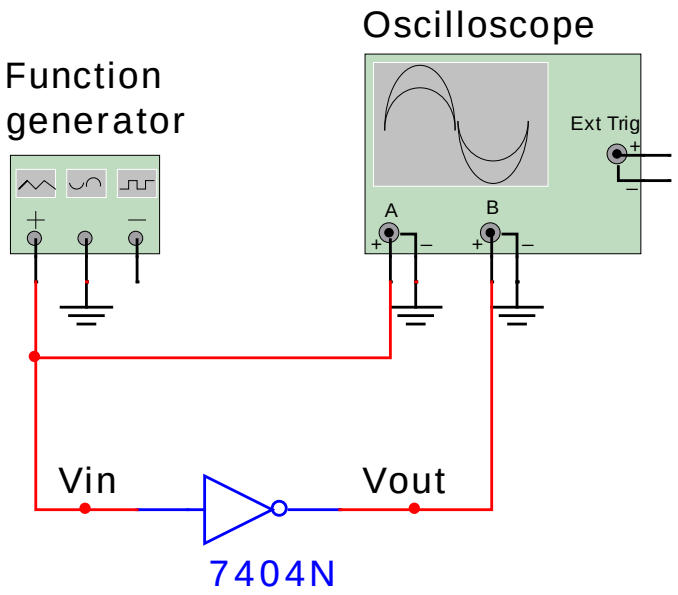
Propagation times

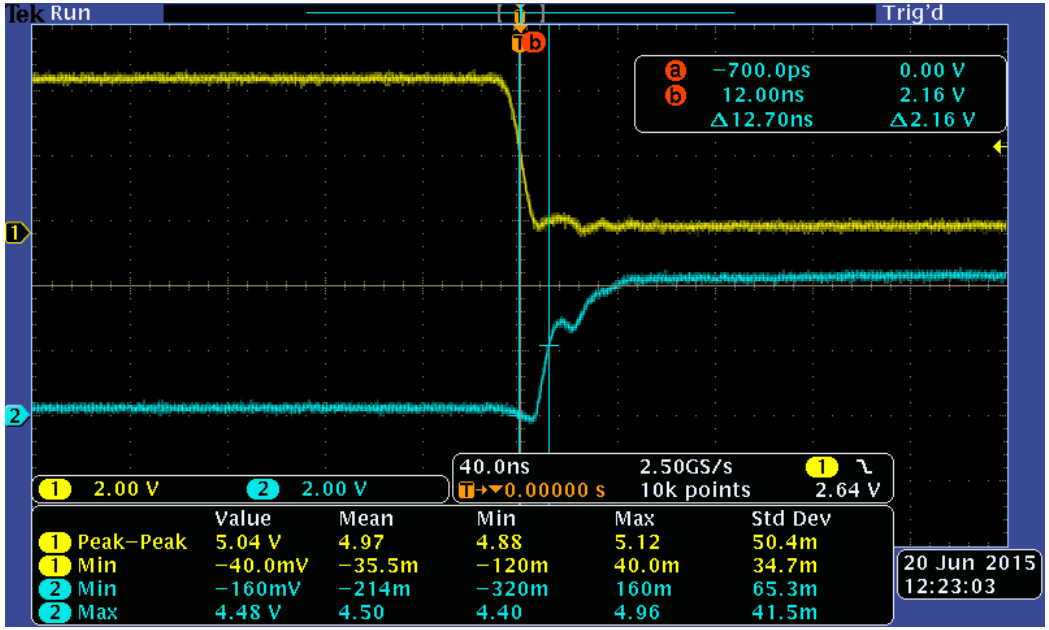




t_{PHL} (High to low)

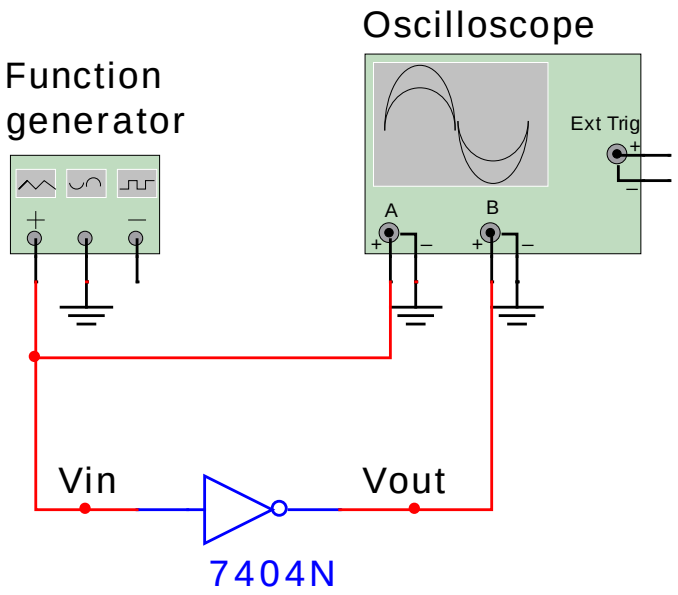
Propagation times

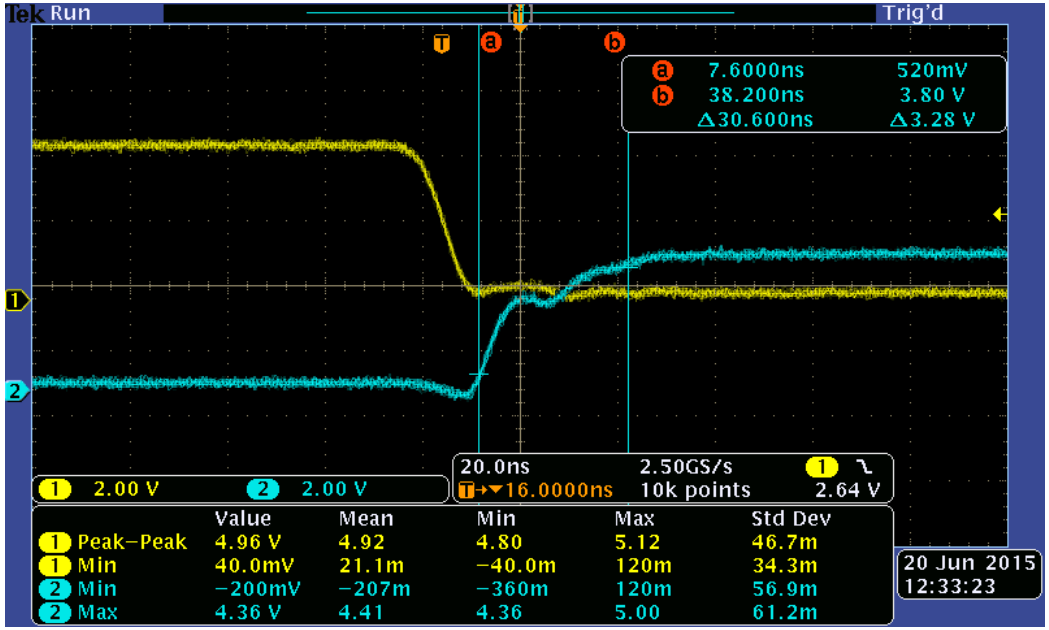




t_{PLH} (Low to high)

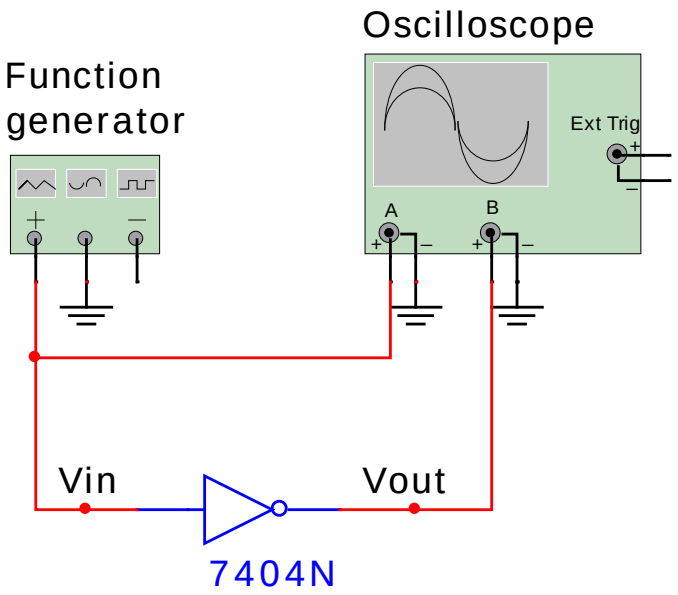
Rise time

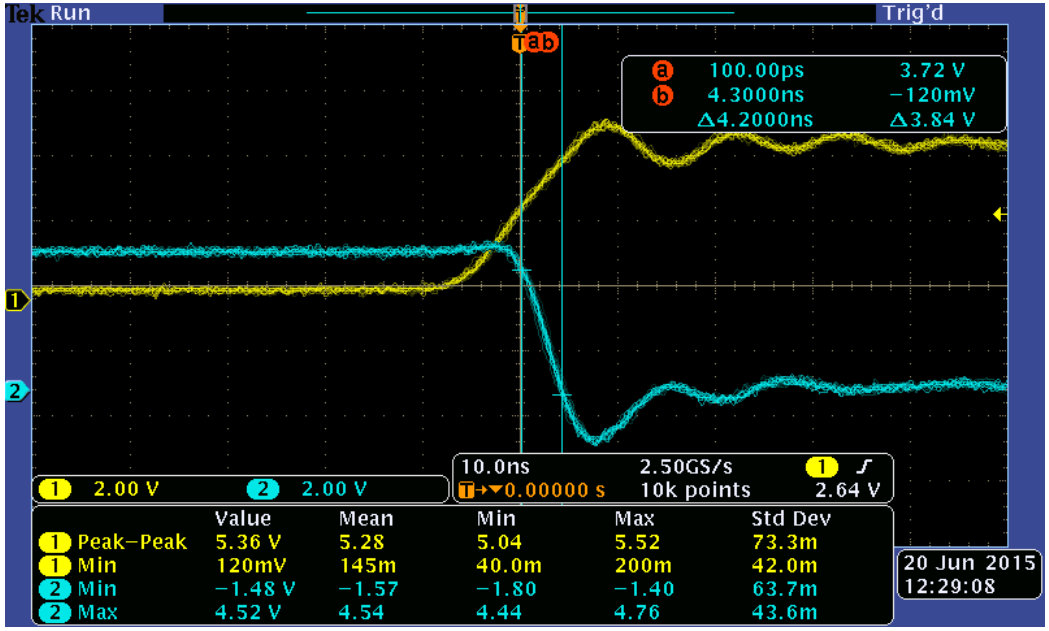




t_{RISE}

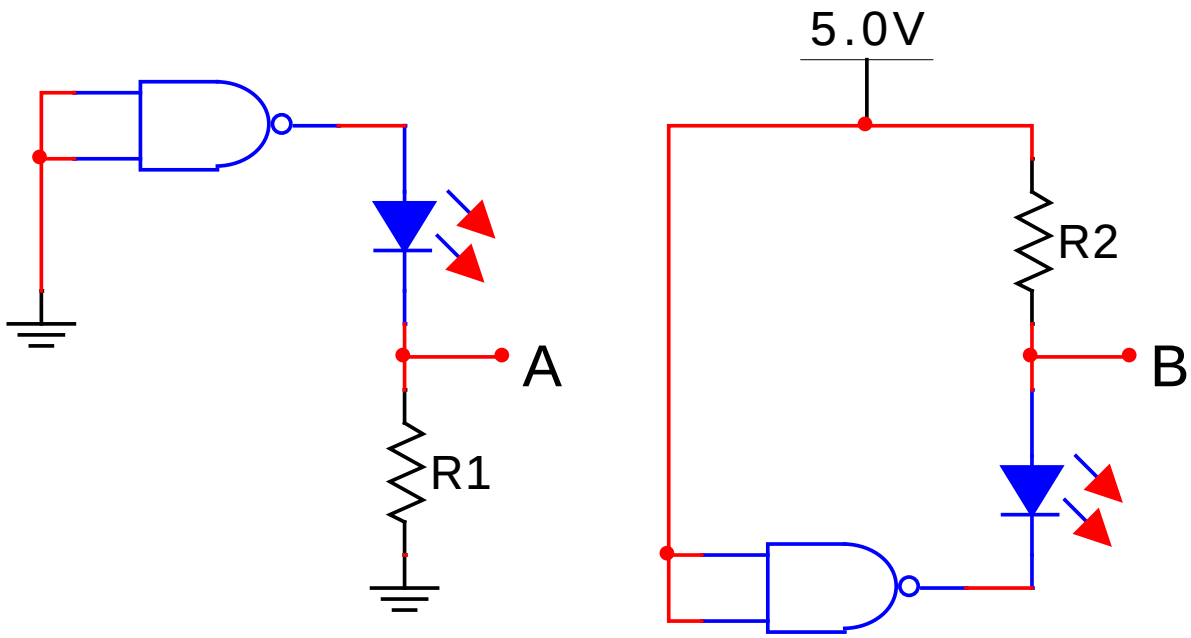
Fall time



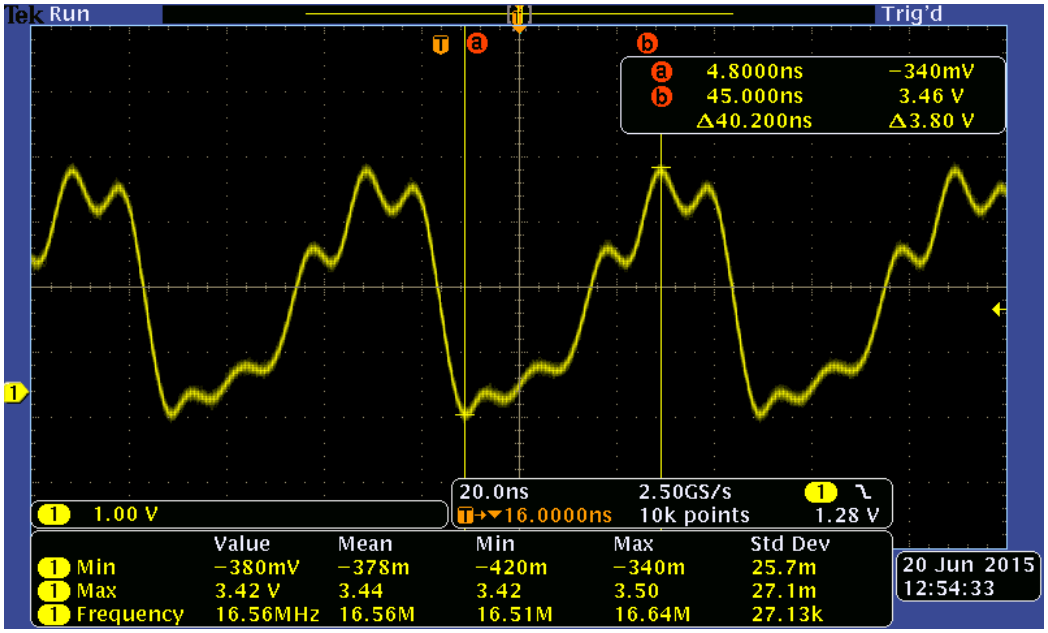


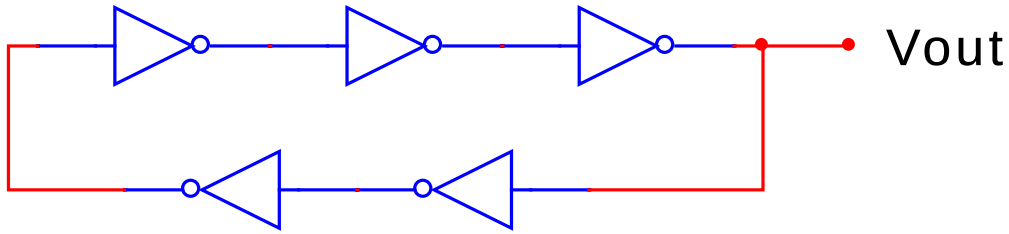
t_{FALL}

Active high vs. active low

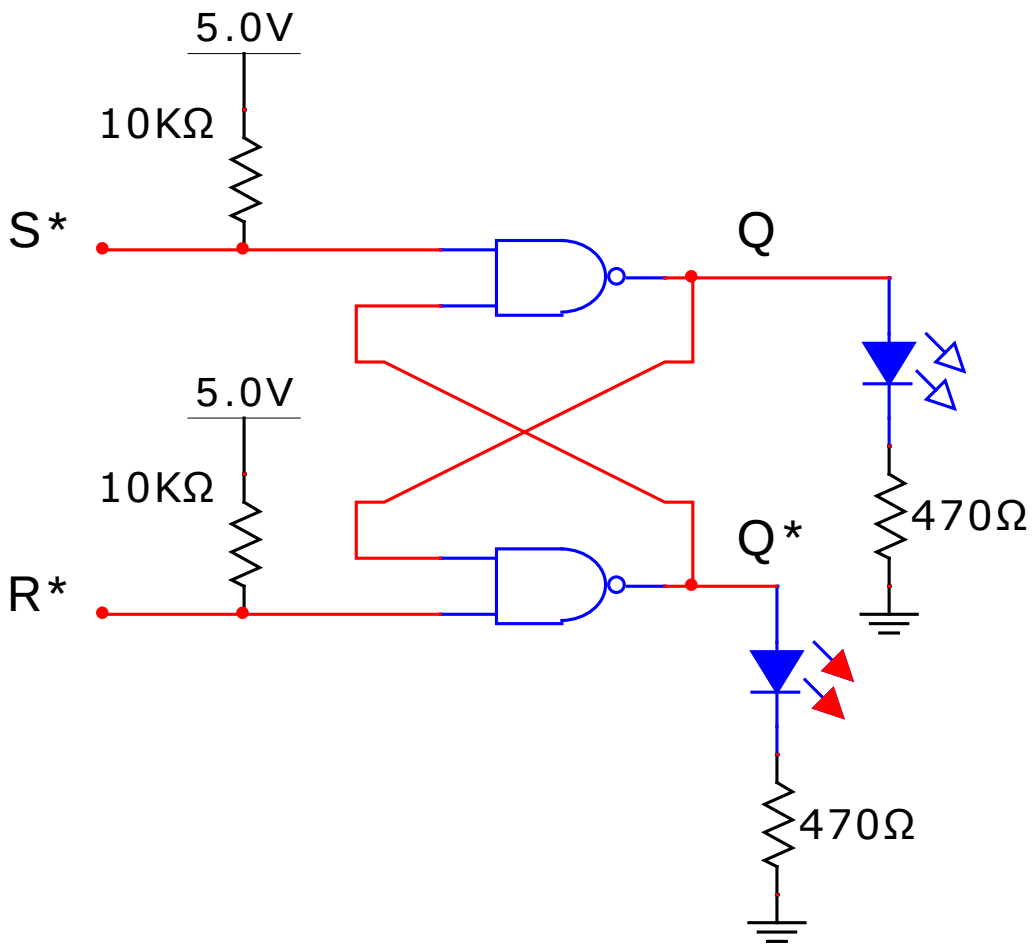


Ring oscillator

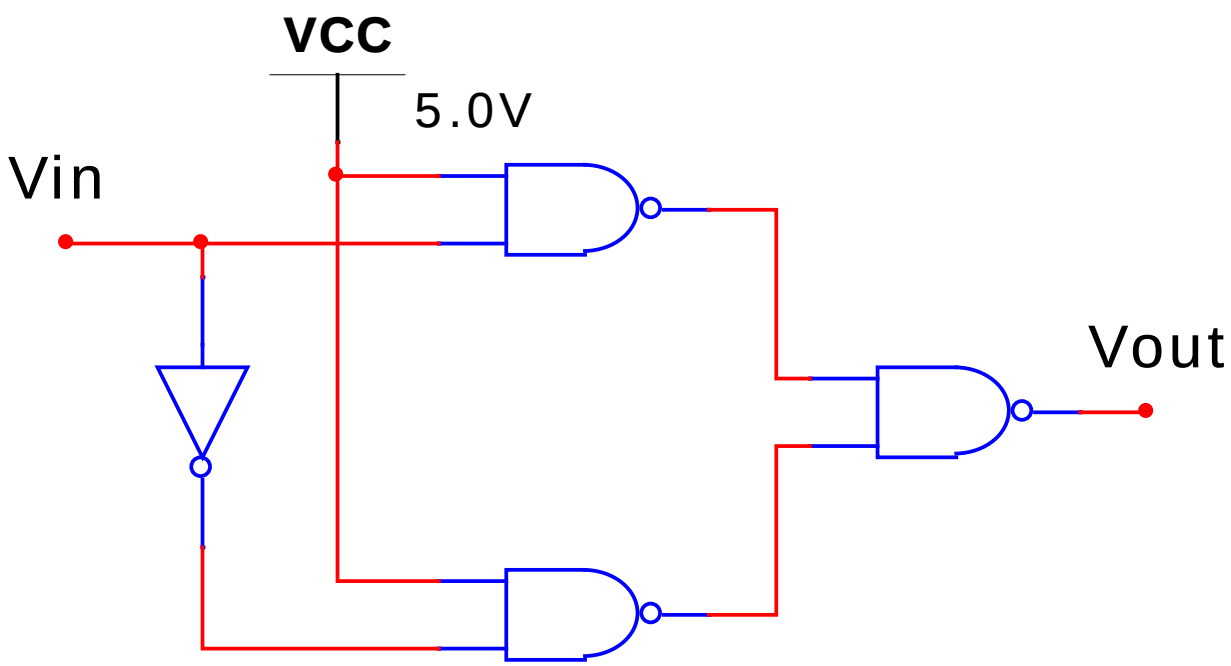




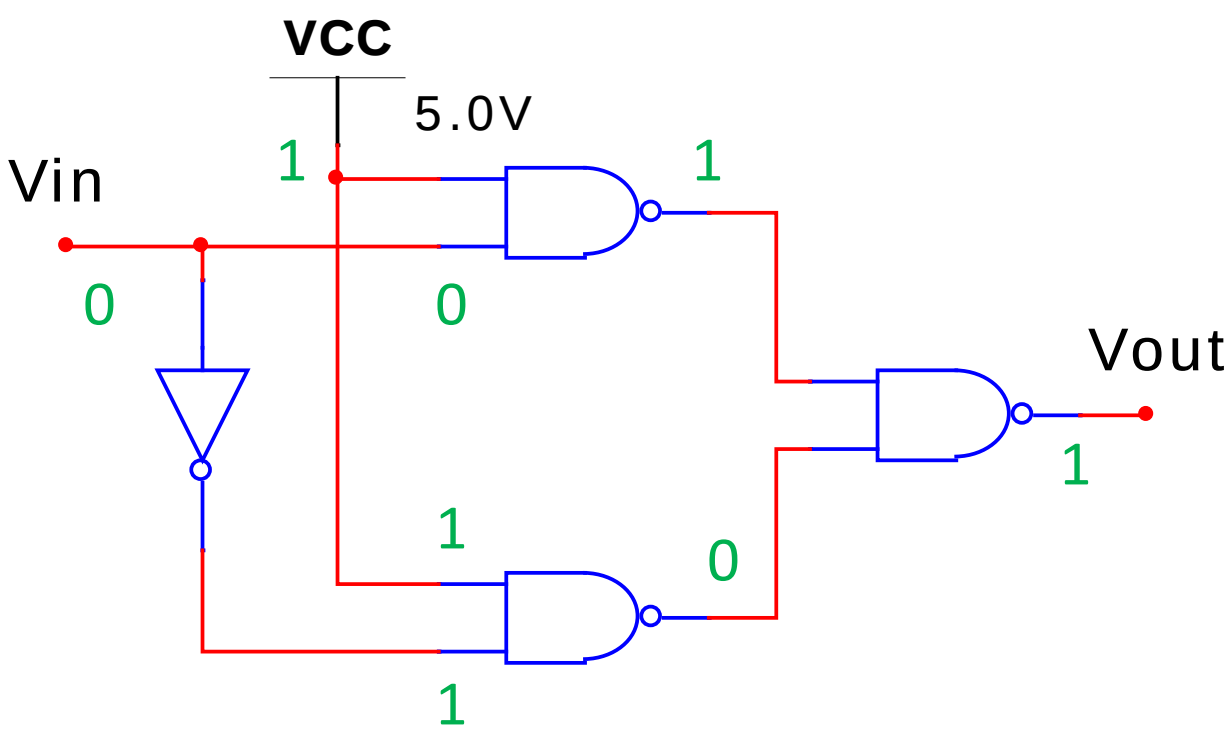
Set/reset latch



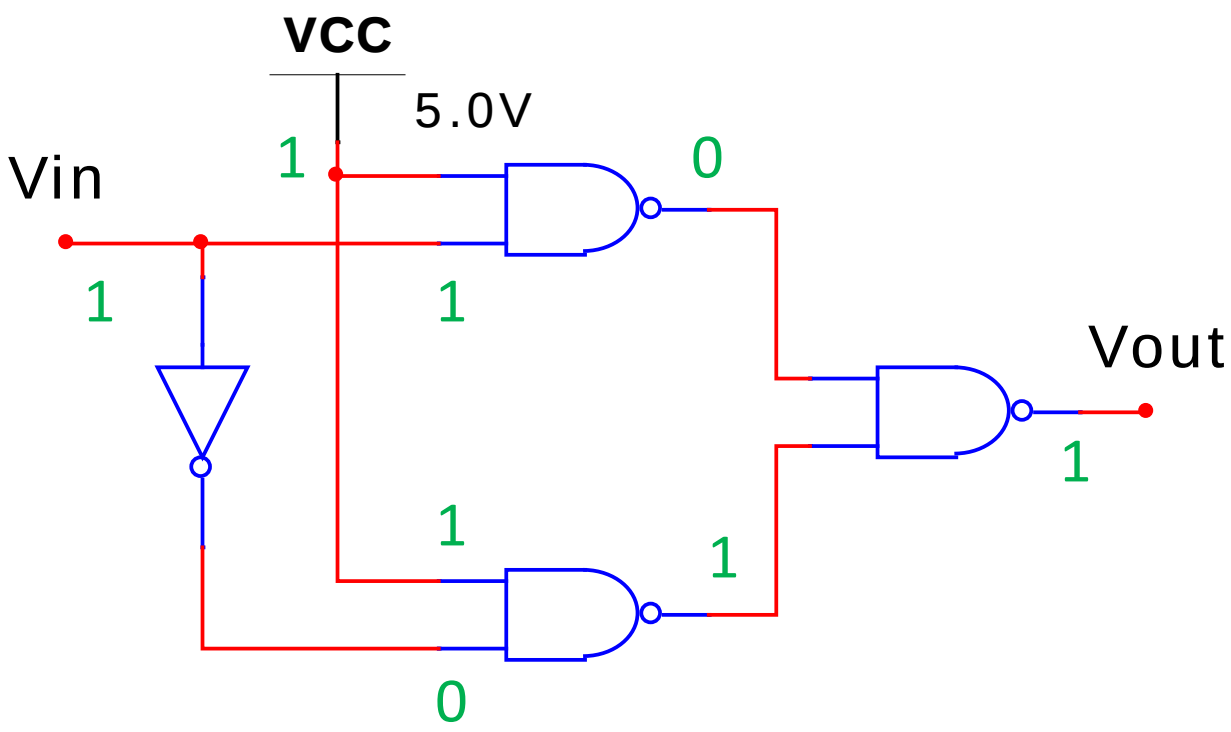
A circuit with a hazard

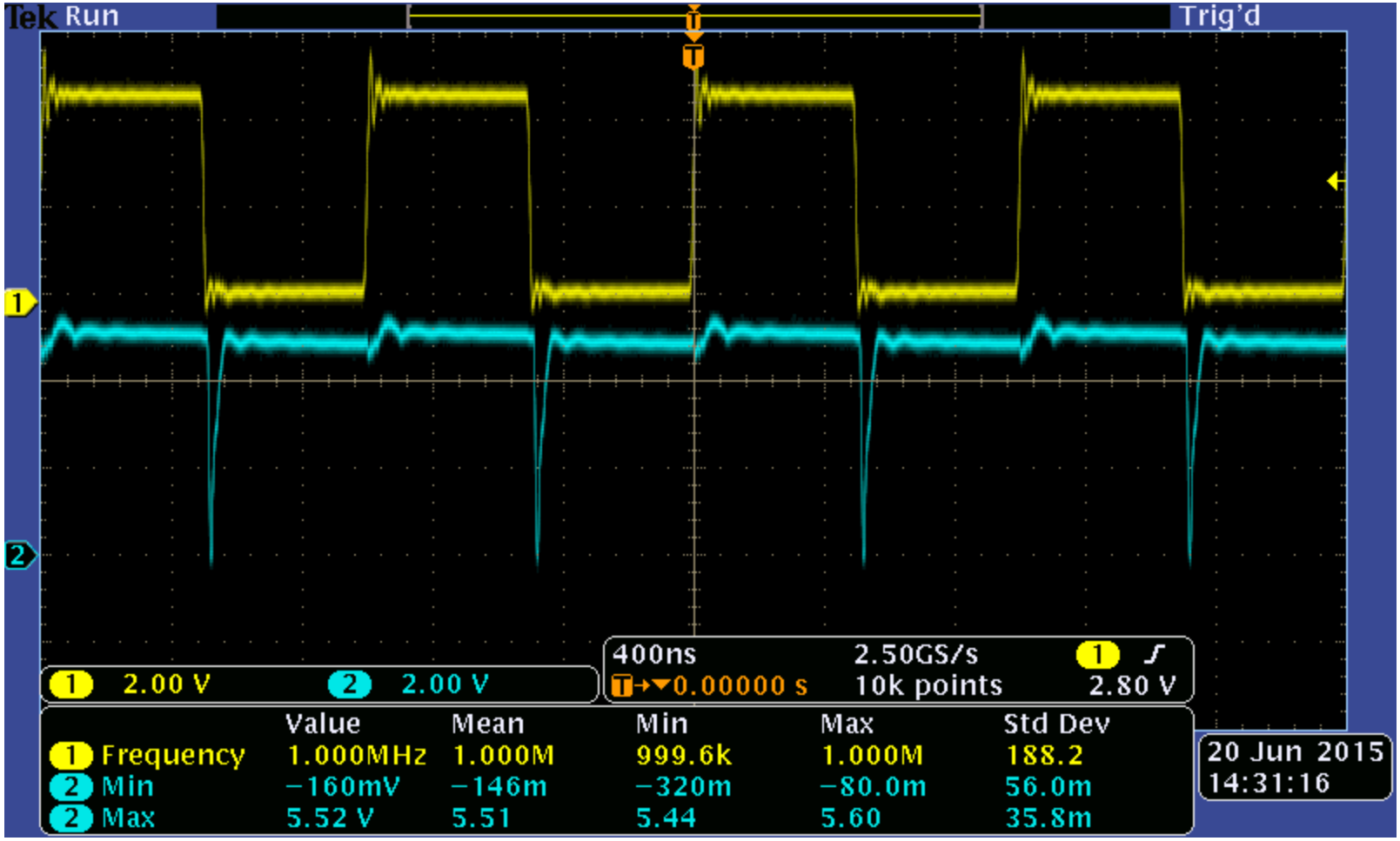


If Vin = 0, Vout = 1

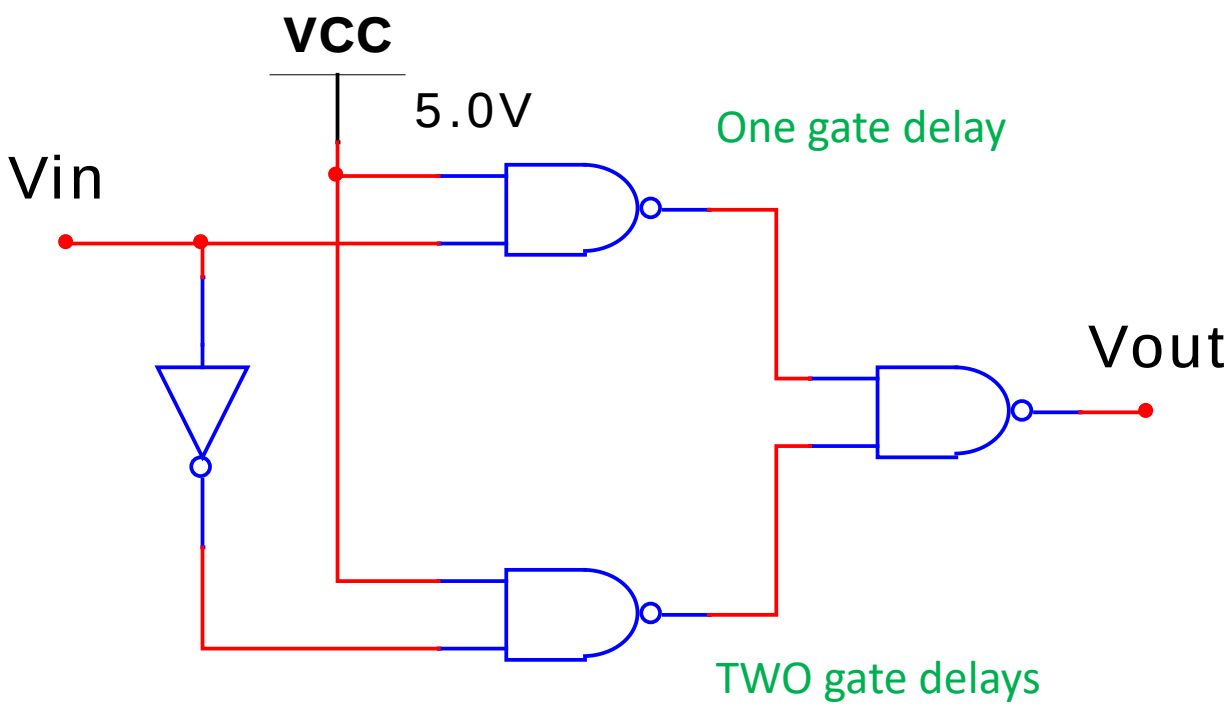


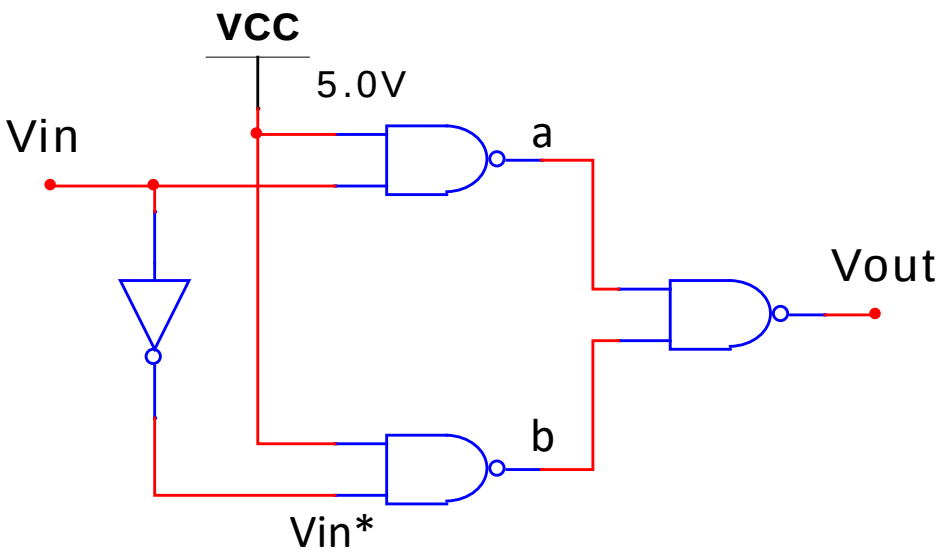
If Vin = 1, Vout = 1 (same)

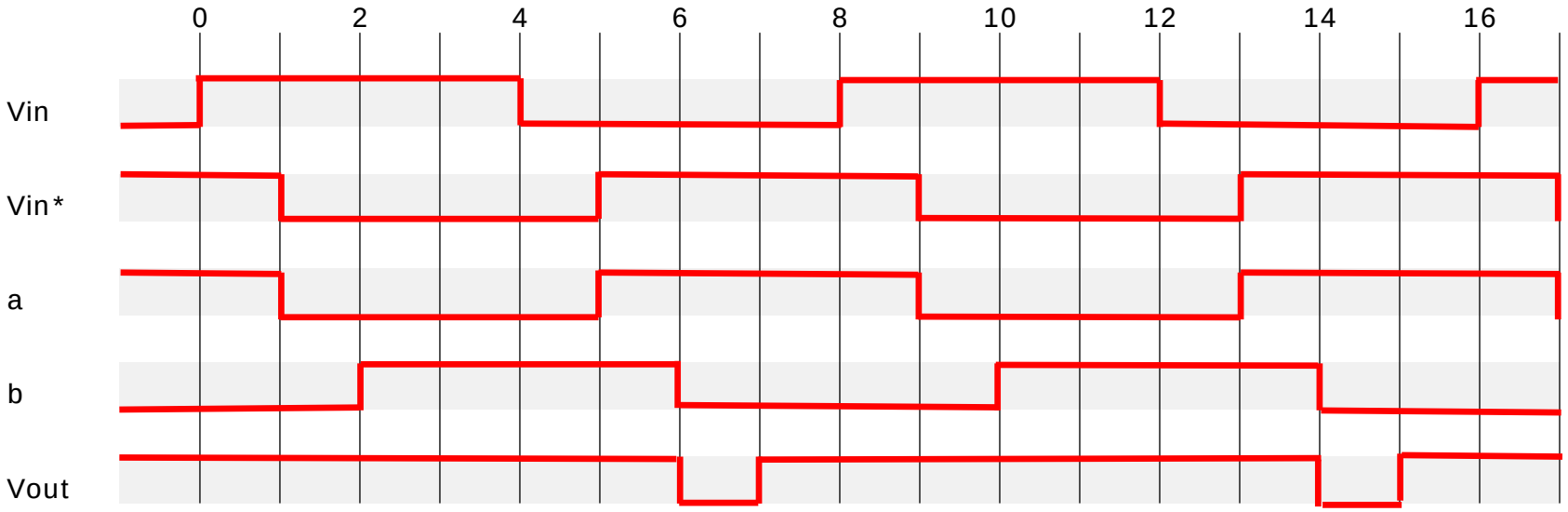



Tek Run
Trig'd
1
2
1 2.00 V
2 2.00 V
400ns
2.50GS/s
1
0.00000 s
10k points
2.80 V
Value Mean Min Max Std Dev
1 Frequency 1.000MHz 1.000M 999.6k 1.000M 188.2
2 Min −160mV −146m −320m −80.0m 56.0m
2 Max 5.52 V 5.51 5.44 5.60 35.8m
20 Jun 2015
14:31:16

A circuit with a hazard




VCC
5.0V
Vin
a
Vout
b
Vin*


0
2
4
6
8
10
12
14
16
Vin
Vin*
a
b
Vout